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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/702,593	10/31/2000	Cary A. Coutant	10001275-1	1046

22879 7590 06/02/2005

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EXAMINER

KENDALL, CHUCK O

ART UNIT PAPER NUMBER

2192

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/702,593

Applicant(s)

COUTANT ET AL.

Examiner

Chuck Kendall

Art Unit

2192

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 March 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is in response to the application filed 3/07/05.
2. Claims 1 – 16 are pending.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Davidson et al. USPN 5,613,117 (hereinafter Davidson).

Regarding claims 1 & 16, Davidson anticipates a computer-implemented method, and a computer program for switching between multiple implementations of a routine in a library of routines that are linked with an application program that is hosted by a computer system (5: 55 – 60), comprising:

compiling a plurality of implementations of a routine into respective object code modules, the routine having an associated name and each implementation adapted to a selected hardware configuration (for plurality of implementations see 5: 45 – 50 & 6: 22 – 40, and 6: 57 – 67, shows (adapting) customizing));

associating the object code modules with the name of the routine and respective sets of hardware characteristics (9:8 – 15, also see 6:30 - 50); and

resolving when the application program is loaded into memory of the computer system, a reference to the routine using the sets of hardware characteristics and a hardware configuration of the system (27:23 – 32, see RISC, CISC and little endian bit ordering regarding hardware characteristics and configuration).

Regarding claim 2, the method of claim 1, further comprising establishing a symbol table having a plurality of entries, each entry including a name of a routine and a reference to an object code module in the library (28:65 – 67, see variable and label for symbolic table 30).

Regarding claim 3, the method of claim 2, further comprising, for the routine having a plurality of implementations, adding a plurality of entries to the symbol table and associating respective sets of hardware characteristics with the plurality of entries (28:55 – 67, see variable and label for symbolic table 30, for hardware characteristics, see 27: 23 - 33).

Regarding claim 4, the method of claim 3, wherein the hardware characteristics include at least one of clock speed of the processor, processor model, cache configuration of the system, hardware operation latency times, instruction set characteristics, bypass characteristics, branch prediction behavior, pre-fetching capability, information describing stall conditions, branch penalties, size and associativity of processor data structures, queue sizes for out-of-order or decoupled processors, and the number of processors in a multiprocessor system (27: 23 – 33, see 32 bit RISC machine, also see CISC).

Regarding claim 5, the method of claim 4, wherein the resolving step further comprises obtaining the hardware configuration of the system from at least one of a system configuration data file, one or more system identification registers, and system firmware (6: 43 – 47).

Regarding claim 6, the method of claim 3, wherein the resolving step further comprises obtaining the hardware configuration of the system from at least one of a system configuration data file, one or more system identification registers, and system firmware (6: 43 – 48, see register set).

Regarding claim 7, the method of claim 1, wherein the hardware characteristics include at least one of clock speed of the processor, processor model, cache configuration of the system, hardware operation latency times, and instruction set characteristics (6:47, see specific instruction set).

Regarding claim 8, the method of claim 1, wherein the resolving step further comprises obtaining the hardware configuration of the system from at least one of a system configuration data file, one or more system identification registers, and system firmware (6: 43 – 48, see register set).

Regarding claim 9, a computer-implemented method for switching between multiple implementations of a routine in a library of routines that are linked with an application program hosted by a computer system, comprising:

- establishing a set of hardware configuration characteristics that describe the computer system (6: 43 – 48, see register set);

- establishing a symbol table, the symbol table having one or more entries that include a name of a routine, a set of hardware characteristics, and an address referencing a routine in the library (9: 8 – 15);

- obtaining a name of a routine having multiple implementations when the library is loaded with the application program into memory of the computer system (28:65 – 67, see variable and label for symbolic table 30);

- matching the name of the routine and the set of hardware configuration characteristics that describe the computer system to an entry in the symbol table (9:20 – 30); and

- generating an address in executable code for references to the routine having multiple implementations when the library is loaded with the application program, the address referencing an implementation in the library as identified in the matching step by the entry in the symbol table (6:47 – 50, see specific addressing).

Regarding claim 10, the method of claim 9, wherein the hardware configuration characteristics include at least one of clock speed of the processor, processor model, cache configuration of the system, hardware operation latency times, and instruction set Characteristics (27: 23 – 33, see 32 bit RISC machine, also see CISC)

Regarding claim 11, the method of claim 10, wherein the resolving step further comprises obtaining the hardware configuration of the system from at least one of a system configuration data file, one or more system identification registers, and system firmware (6: 43 – 48, see register set).

Regarding claim 12, the method of claim 9, wherein the resolving step further comprises obtaining the hardware configuration of the system from at least one of a system configuration data file, one or more system identification registers, and system firmware (6: 43 – 48, see register set).

Regarding claim 13, which discloses the apparatus version of claim 1, see reasoning as previously discussed above.

Regarding claim 14, Davidson anticipates a computer-implemented symbol table for referencing a library of object code modules that implement a plurality of routines, comprising:

a first set of one or more entries, each entry in the first set including a unique name of a routine and a reference to an object code module in the library (28:55 – 67, see variable and label for symbolic table 30, for hardware characteristics, see 27: 23 - 33); and

a second set of one or more entries, each entry in the second set including a shared name of a routine, a set of hardware characteristics, and a reference to an object code module in the library (29: 1 – 5, see literal table).

Regarding claim 15, the symbol table of claim 14, wherein the hardware characteristics include at least one of clock speed of the processor, processor model, cache configuration of the system, hardware operation latency times, instruction set characteristics, bypass characteristics, branch prediction behavior, pre-fetching capability, information describing stall conditions, branch penalties, size and associativity of processor data structures, queue sizes for out-of-order or decoupled processors, and the number of processors in a multiprocessor system (27: 23 – 33, see 32 bit RISC machine, also see CISC).

Response to Arguments

5. Applicant's arguments filed 03/07/02 have been fully considered but they are not persuasive.

Applicant argues (1) on page 6 of Applicants response that Davidson doesn't disclose "associating object modules with the name of the routine and respective sets of hardware characteristics".

Applicant also argues (2) that Davidson does not teach "resolving when the application program is loaded into memory... a reference to the routine using the sets of hardware characteristics".

Applicant argues (3), that in claim 3, Davidson does not teach having a plurality of implementations, a plurality of entries are added to the symbol table and respective set of hardware characteristics are associated with the plurality of entries.

Applicant also argues (4) in claim 5 that Davidson doesn't disclose "including obtaining the hardware configuration of the system from at least one of a system configuration data file.

Regarding arguments in claim 9, Applicant simply rehashes arguments from claim 1, which have been previously discussed above.

Regarding claim 14, rehashes arguments from claim 3 which has been discussed above, in arguments section.

Response (1), Examiner disagrees in 6:30 – 50, Davidson discloses generating target object code from the internal representation (characteristics) and routines are then provided by the back end to obtain language specific information (associating) object module with back end routines, and furthermore the code being created for the target machine (object code) has a specific architecture and register set (hardware characteristics).

Response (2) and with regards to resolving when load in memory a reference using the sets of hardware characteristics, Davidson teaches in 27:23 – 32, the compiler being able to address (resolve) a variety of architectures with regards to the different hardware configurations (characteristics), Examiner interprets this to be equivalent to Applicant's claimed limitations.

Response (3), regarding Applicant's argument that Davidson doesn't teach a plurality of entries added into the symbol table and respective set of characteristics are associated with the plurality of entries, Examiner believes that Davidson does in fact disclose this. Davidson in 27:22 – 25, teaches " a symbol table in particular, is intended to address a variety of architectures ranging from...(CISC) such as VAX to ...(RISC).:", Examiner believes that it is inherent for the table to have a plurality of entries and respective set of characteristics of the symbol associated with the respective hardware characteristics of a CISC or RISC processor.

Regarding (4), regarding Applicant's argument in claim 5, Examiner also believes that the symbol table which is intended for address different architectures would in fact being able obtain language specific information which Examiner has interpreted to be equivalent to configuration information. (6:37 – 43).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuck Kendall whose telephone number is 571-272-3698. The examiner can normally be reached on 10:00 am - 6:30pm.

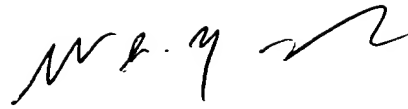
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ck.

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A handwritten signature in black ink, appearing to read 'Wei Y. Zhen', with a stylized flourish at the end.

WEI Y. ZHEN
PRIMARY EXAMINER